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EXAMINER	
CHANG, EDITH M	

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2634	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/436,522	SHA ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 9-10, filed December 22 2003, with respect to the rejection(s)of claim(s) 1 and 4-21 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-5, 8-10, 13-15, & 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hardin (US Patent 5631920).

Regarding **claims 1 & 13-14** Harding et al. discloses a spread spectrum clock generator circuit and its method (FIG.7) comprising: a first circuit/means (50-60 FIG.7) configured to generate a clock signal (68 FIG.7) in response to (i) a reference signal (50 FIG.7, column 7 lines 33-37), (ii) a sequence of spread spectrum ROM codes (56 FIG.7, column 7 lines 16-21), and (iii) a command signal (54 FIG.7, column 7 lines 37-38), wherein (i) the clock signal is spread spectrum modulated (the 68 FIG.7 is the spread spectrum modulated clock signal) and (ii) the spread spectrum modulation of the clock signal can be switched on and off in response to the

command signal (54 FIG.7, column 7 lines 40-52, wherein the command signal reset the counter to switch on and off the modulated clock signal); and a second circuit/means (52-70 FIG.7) to synchronize the command signal (54, 52, 58 FIG.7, column 7 lines 45-52 where the command signal can change the ROM code provided to the feedback signal) to a feedback signal (68, 70, 62 FIG.7, column 7 lines 53-56 & lines 63-67), wherein the sequence of spread spectrum ROM code is predetermined mathematical formula (column 4, lines 39-44, column 5 lines 12-column 6 line 20, the frequency deviation is the formula) and optimized in accordance with predetermined criteria (column 4 lines 44-46, lines 49-52, the EMI components/harmonic amplitudes, etc. set the criteria in the profile, FIG.2-5).

Regarding **claim 4**, Hardin discloses the apparatus is used with a motherboard or CPU (column 2 lines 59-63).

Regarding **claims 5 & 19**, Hardin discloses the second circuit and the method to generate one or more control signals (64 & 58 FIG.8, column 8 lines 51-58) in response to (i) the command signal (54 FIG.8), and (ii) the feedback signal (68 FIG.8) to synchronize the command signal to the feedback signal.

Regarding **claim 8**, Hardin discloses the predetermined criteria are applied to the clock signal during a transition period when spread spectrum modulation is switching on or switching off (column 7 lines 15-21, the modulation variation values stored in ROM provide the predetermined criteria to the clock signal/68 FIG.7 during a transition, in Abstract the harmonic/EMI components where during the transition period is).

Regarding **claims 9 & 10**, Hardin discloses a predetermined minimum frequency and a predetermined maximum frequency for the clock signal (column 1 lines 25-34 where the

minimum and maximum frequencies predetermined for microprocessor, column 2 lines 25-30 where Harding discloses the clock signal for microprocessor, column 3 lines 10-20).

Regarding **claim 15**, Harding discloses steps of selecting a number of ROM codes according to predetermined mathematical formula to generate a spread spectrum modulation signal (FIG.7, column 5 line 12-column 6 line 24, where the code in 56 is selected according to formula to generate a spread spectrum modulation signal 68 FIG.7).

Regarding **claim 18**, Hardin discloses controlling a feedback divider (52 FIG.8) with the sequence of spread spectrum ROM codes (56 FIG.8).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardin (US Patent 5631920) in view of Marten et al. (US 6590949 B1).

Regarding **claims 6-7, & 20**, Hardin does not specify the latch, further Marten et al. teaches a first latch and a second latch in the phase detector (30 & 32 FIG.2, column 2 lines 40-45). As Hardin using the phase detector in the second circuit (62 FIG.7/FIG.8), at the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the phase detector having one or more latches used taught by Marten et al. in Hardin's second circuit

to create control signals and to reduce the drift in phase when the reference clock signal fails (column 1 lines 57-62).

6. Claims 11-12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardin (US Patent 5631920) in view of Hardin et al. ("Design considerations of phase-locked loop systems for spread spectrum clock generation compatibility", IEEE 1997 IS on EC, 18-22 Aug.1997).

Regarding **claim 11**, further Hardin et al. (IEEE 1997) teaches the predetermined mathematical formula cited in the claim (page 304 left column equation (1) wherein the I_{CP} is the CP, the current form of the charge pump as shown in Figure 3 on page 303, N_{FB} is the FDB, etc.). Both mathematical formulae are derived from the same model, Figure 3 of Hardin et al. (IEEE 1997) as the FIG.5 of the instant application. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the mathematical formula derived from the same model taught by Hardin et al. (IEEE 1997) to analyze the timing parameters of PLL to reduce the EMI /radiated emission (page 306 Conclusions).

Regarding **claim 12**, further Harding et al. (IEEE 1997) teaches the sequence of spread spectrum ROM codes is optimized using a computer program to simulate transient behavior apparatus (page 304 right column the last paragraph, page 305 left column second paragraph, Figure 5 is the simulated results).

Regarding **claim 21**, except explicitly specify the simulated transient behavior, Harding discloses an apparatus comprising: a first circuit/means (FIG.7 50-60) configured to generate a clock signal (FIG.7 68) in response to (i) a reference signal (FIG.7 50), (ii) a sequence of spread

spectrum ROM codes (FIG.7 56), and (iii) a command signal (FIG.7 54); and a second circuit/means (FIG.7 52-70) configured to synchronize the command signal to a feedback signal (FIG.7 68) wherein the sequence of spread spectrum ROM codes is generated and optimized using a computer program to simulate transient behavior of the apparatus (Abstract where the reduce the harmonic/EMI spectral components) wherein the sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula (column 4 lines 39-44, column 5 line 12-column 6 line 20) and optimized in accordance with predetermined criteria (column 4 lines 44-46, lines 49-52). Further Harding et al. (IEEE 1997) teaches the sequence of spread spectrum ROM codes is optimized using a computer program to simulate transient behavior apparatus (page 304 right column the last paragraph, page 305 left column second paragraph, Figures 5-8, and tables are the simulated results). As Harding using the apparatus to reduce the harmonic/EMI spectral components (Abstract, where harmonic/EMI components as the transient behaviors that the simulation needed to perform), at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the teaching taught by Hardin et al. (IEEE 1997) in Hardin's method to analyze and simulate the timing parameters of PLL to reduce the EMI /radiated emission (page 306 Conclusions).

7. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardin (US Patent 5631920) as applied to claim 15 above, further in view of Hardin et al. ("Design considerations of phase-locked loop systems for spread spectrum clock generation compatibility", IEEE 1997 IS on EC, 18-22 Aug.1997) and Young et al. (A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors, Solid-State Circuits, IEEE Journal of, Volume: 27, Issue:11, Nov. 1992).

Regarding **claim 16**, Harding discloses (A) initializing a PLL; (B) stabilizing the PLL with spread spectrum modulation turned off (A & B are the part of the initializing procedure of the SSCG with PLL provided by FIG.7, column 8 lines 44-47 where the 66 is a VCO); (C) loading the sequence of spread spectrum ROM code; (D) switching on spread spectrum modulation (steps A-D are the steps of operating the SSCG with PLL system FIG.7 in order to get the transient behavior to reduce the harmonic/EMI components stated in Abstract, column 4 lines 15-21); the steps of recording (E)-(K) (FIG.2-5, providing the plots of clock output according to with modulation profiles performs the recording steps of the transient behavior, the turn on and off the spread spectrum modulation are part of the steps to have the transient behavior created in order to reduce the harmonic/EMI component where the transient behavior obtained, Abstract), wherein step (H) comparing recorded transient behavior to predetermined criteria (column 6 lines 30-32 where comparing performs); step (I) if the recorded transient behavior does not meet the predetermined criteria, shifting the sequence of spread spectrum ROM code, wherein a last ROM code is moved to a first position and remaining ROM codes are shifted one position forward (column 7 lines 39-50 where the counters performs the step).

Further Hardin et al. teaches/illustrates the (E) recording transient behavior of the clock signal till PLL is in spread spectrum steady-state (F) switching off spread spectrum modulation; (G) recording transient behavior of the clock signal until spread spectrum modulation is completely off; (J) if the recorded transient behavior meets the predetermined criteria, finalizing the sequence of spread spectrum codes (page 303 right column lines 32-33, page 304 right column the last paragraph, Figure 6, 7, & 8, page 306 right column Conclusions section lines 4-8 where the transient behavior recorded, compared, shifting the ROM codes changing the profile,

simulated and the result get); and (K) repeating sub-steps (D) through (J) until the recorded transient response meets the predetermined criteria (page 306 left column the last paragraph, the Time Interval Analyzer performs the recording and repeating steps (D) to (J) to provide multiple recordings/values to compose the simulated results in Figures 6-8, and Tables 1-2) . As Harding's method reducing the harmonic/EMI components to provide the measurement of the output clock of the SSCG system, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the steps of recording the output clock of the SSCG with PLL taught by Hardin et al. (IEEE 1997) in Hardin's method to analyze the timing parameters of PLL to reduce the EMI /radiated emission (page 306 Conclusions).

Further, Young et al. teaches the PLL characteristics (initializing a PLL at power supply ramping in the clock generator (page 1601 section IV.). As the Harding using the PLL in the clock generator, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the PLL characteristics taught by Young et al. in Harding's method to initializing and stabilizing the PLL to have a PLL-based deskewed clock generator (page 1599 right column the first paragraph).

Regarding **claim 17**, Harding discloses the steps performed by a computer program (1 FIG.1, column 8 lines 59-67), further Harding et al. discloses the sub-steps performed by a computer program (Figure 1, Microprocessor, System Logic and Chip Sets) as well.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
February 20, 2004

CHIEH M. FAN
PRIMARY EXAMINER